What is claimed is:

1. A liquid crystal display device for receiving horizontal and vertical synchronization signals and at least one analog video signal synchronized with said horizontal synchronization signal from a host and displays an image on a screen thereof, said LCD device comprising:

a display mode discriminating means for discriminating a display mode supported by said host in response to said horizontal and vertical synchronization signals to generate first and second mode signals and first, second, third and fourth data signals related to said discriminated display mode;

a clock generator for generating first and second pixel clock signals in synchronization with said horizontal synchronization signal, said first and second pixel clock signals having frequencies corresponding to said first and second data signals, respectively, a pulse number of said first pixel clock signal corresponding to one horizontal line being equal to a value of said first data signal and a pulse number of said second pixel clock signal corresponding to one horizontal line being equal to a value of said second data signal;

an analog-to-digital converter for converting said at least one analog video signal into a digital video signal in synchronization with said first pixel clock signal;

a memory for storing said digital video signal;

a horizontal output generator for receiving said third and fourth data signals in response to said vertical synchronization signal and generating a horizontal output signal, said digital video signal being read from said memory in synchronization with said horizontal output signal, a pixel number per one cycle of said horizontal output signal being equal to a value of said third data signal, and a pixel number per a pulse width of said horizontal output signal being equal to a value of said fourth

data signal; and

a memory controller for enabling said digital video signal to be stored in said memory in accordance with said first and second mode signals, said horizonal synchronization signal and said first pixel clock signal, and enabling said digital video signal stored in said memory to be read from said memory in accordance with said second mode signal, said horizontal output signal and said second pixel clock signal.

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2. The light crystal display device as set forth in claim 1, wherein said memory comprises:

first, second and third memory blocks corresponding to red, green, and blue data of said digital video signal, each of said memory blocks having at least three line memories, wherein each of said line memories stores said corresponding red, green and blue data of said digital video signal from said ADC and corresponding to one horizontal line; and

first, second and third multiplexers for selectively outputting data from each of said line memories of corresponding ones of said memory blocks in response to a data selection signal from said memory controller.

3. The light crystal display device as set forth in claim 2, wherein said memory controller comprises:

a flag generator for generating a plurality of write flag signals and a plurality of read flag signals;

a memory selector for generating said first and second memory selection signals for selecting said line memories in response to said write and read flag signals to block simultaneous read and write

operations of a same one of said line memories; and

a memory operation control circuit for controlling write and read access to said line mories in each of said memory blocks in response to said horizontal synchronization signal, said horizontal output signal, said first memory selection signal and said first and second pixel clock signals.

4. The light crystal display device as set forth in claim 1, wherein said memory, said horizontal output generator and said memory controller are constituted by a single chip.

5. A video signal converting apparatus which is provided to convert a first display signal of serial format into a second display signal of parallel format, said apparatus comprising:

means for detecting a first resolution signal indicative of a resolution of said first display signal using horizontal and vertical synchronization signals related to said first display;

means for comparing said first resolution signal with a second resolution signal indicative of a reference resolution; and

means for converting said first display signal into said second resolution signal, if there is a difference between said first and said second resolution signals.

6. A display apparatus which receives horizontal and vertical synchronization signals, and a video signal of serial format synchronized with said horizontal synchronization signal from a host, and displays an image on a screen composed of a plurality of horizontal lines, each of said horizontal lines having a plurality of pixels, said display apparatus comprising:

means for detecting the pixel number corresponding to said video signal from said host using

said horizontal and vertical synchronization signals;

means for comparing the pixel number with a reference pixel number; and

means for sampling said video signal using a first frequency clock generated in accordance with a difference between the pixel number and the reference pixel number; and

means for displaying said sampled video signal on said screen in synchronization with a second frequency clock generated in accordance with said difference.

7. The display apparatus of claim 6, wherein said sampling means comprises a first clock generator for generating said first frequency clock synchronized with said horizontal synchronization signal in response to a first data signal from said detecting means, the pulse number of said first frequency clock corresponding to one horizontal line being equal to a value of said first data signal, and a converter for converting said video signal of serial format into a video data signal of parallel format.

8. The display apparatus of claim 6, wherein said displaying means comprises a second clock generator for generating said second frequency clock synchronized with said horizontal synchronization signal in response to said first data signal, the pulse number of said first frequency clock corresponding to one horizontal line being equal to a value of said first data signal, and a horizontal output generator for generating a horizontal output signal in response to second and third data signals from said detecting means, said sampled video signal being synchronized with said horizontal output signal.

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9. The display apparatus of claim 6, further comprising a converter said sampled video signal into a data signal corresponding to the number of said horizontal lines in accordance with a predetermined ratio determined by said difference between the pixel number and the reference pixel number, said data signal being provided to said displaying means.

10. A video signal converting apparatus for converting an analog video signal into a digital video signal, said apparatus comprising:

a memory for storing said digital video signal;

a horizontal output generator for receiving first and second data signals in response to a vertical synchronization signal and generating a horizontal output signal, said digital video signal being in synchronization with said horizontal output signal, the pixel number per one cycle of said horizontal output signal being equal to a value of said first data signal, and the pixel number per a pulse width of said horizontal output signal being equal to a value of said second data signal; and

a memory controller for enabling said digital video signal to be stored in said memory.

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